jc595 U.S. PTO 04/16/99

jc511 U.S. PTO 09/292668 04/16/99

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231
Prior Application:

Attorney's Docket Number: 1333.0116-01

Art Unit: 2734

Examiner: D. Vo

SIR: This is a request for filing a

☒ Continuation ☐ Divisional Application under 37 C.F.R. § 1.53(b) of pending prior reissue application Serial No. 08/555,196 filed November 8, 1995 of Paul E. Fleischer and Chi-Leung Lau for SYNCHRONOUS RESIDUAL TIME STAMP FOR TIMING RECOVERY IN A BROADBAND NETWORK.

1. ☒ Enclosed is a complete copy of the prior application including the oath or Declaration and drawings, if any, as originally filed. I hereby verify that the attached papers are a true copy of prior application Serial No. 08/555,196 as originally filed on November 8, 1995.

2. ☐ Enclosed is a substitute specification under 37 C.F.R. § 1.125.

3. ☐ Cancel Claims ______.

4. ☒ A Preliminary Amendment is enclosed.

5. ☒ The filing fee is calculated on the basis of the claims existing in the prior application as amended at 3 and 4 above.

For	Number Filed	Number Extra	Rate	Basic Fee $760.00
Total Claims	5 -20=	0	x$ 18.00=	$ 0.00
Independent Claims	5 -3=	2	x$ 78.00=	156.00
Multiple Dependent Claim(s) (if applicable)			+$260.00=	
			Total =	156.00
		Reduction by ½ for filing by small entity		-
		TOTAL FILING FEE	=	916.00

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09292668 .041599

6. ☒ A check in the amount of $916 to cover the filing fee is enclosed.

7. ☒ The Commissioner is hereby authorized to charge any fees which may be required including fees due under 37 C.F.R. § 1.16 and any other fees due under 37 C.F.R. § 1.17, or credit any overpayment during the pendency of this application to Deposit Account No. 06-0916.

8. ☒ Amend the specification by inserting before the first line, the sentence:

--This is a ☒ continuation ☐ division of reissue application Serial No. 08/555,196, filed November 8, 1995, and claims the benefit of U.S. provisional application no. 60/__________, filed ____________________ ____.-- all of which are incorporated herein by reference.

9. ☐ New formal drawings are enclosed.

10. ☒ The prior application is assigned of record to: Bell Communications Research, Inc.

11. Priority of application Serial No. _________, filed on ________ in ________ ________ (country) is claimed under 35 U.S.C. § 119. A certified copy

☐ is enclosed or ☐ is on file in the prior application.

12. ☐ A verified statement claiming small entity status

☐ is enclosed or ☐ is on file in the prior application.

13. ☐ The power of attorney in the prior application is to at least one of the following: FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P., Douglas B. Henderson, Reg. No. 20,291; Ford F. Farabow, Jr., Reg. No. 20,630; Arthur S. Garrett, Reg. No. 20,338; Donald R. Dunner, Reg. No. 19,073; Brian G. Brunsvold, Reg. No. 22,593; Tipton D. Jennings, IV, Reg. No. 20,645; Jerry D. Voight, Reg. No. 23,020; Laurence R. Hefter, Reg. No. 20,827; Kenneth E. Payne, Reg. No. 23,098; Herbert H. Mintz, Reg. No. 26,691; C. Larry O'Rourke, Reg. No. 26,014; Albert J. Santorelli, Reg. No. 22,610; Michael C. Elmer, Reg. No. 25,857; Richard H. Smith, Reg. No. 20,609; Stephen L. Peterson, Reg. No. 26,325; John M. Romary, Reg. No. 26,331; Bruce C. Zotter, Reg. No. 27,680; Dennis P. O'Reilley, Reg. No. 27,932; Allen M. Sokal, Reg. No. 26,695; Robert D. Bajefsky, Reg.

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14. ☐ The power appears in the original declaration of the prior application.

15. ☐ Since the power does not appear in the original declaration, a copy of the power in the prior application is enclosed.

16. ☒ Please address all correspondence to BELL COMMUNICATIONS RESEARCH, INC., 445 South Street, Morristown, NJ 07960-6438

17. ☐ Recognize as associate attorney ______________________________

____

(name, address & Reg. No.)

18. ☐ Also enclosed is ______________________________

____

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PETITION FOR EXTENSION. If any extension of time is necessary for the filing of this application, including any extension in the parent application, serial no. 08/555,196 , filed November 8, 1995 , for the purpose of maintaining copendency between the parent application and this application, and such extension has not otherwise been requested, such an extension is hereby requested, and the Commissioner is authorized to charge necessary fees for such an extension to our Deposit Account No. 06-0916. A duplicate copy of this paper is enclosed for use in charging the deposit account.

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

By: James K. Hammond
JAMES HAMMOND
Reg. No. 31,964

Date: April 16, 1999

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PATENT
Attorney Docket No. 1333.0116-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Continuation Application of:	)	
Paul E. FLEISCHER ET AL.	)	
Parent Reissue Application Serial No.: 08/555,196	)	Group Art Unit: 2734
Filed: Concurrently	)	Examiner: D. Vo
For: SYNCHRONOUS RESIDUAL TIME STAMP FOR TIMING RECOVERY IN A BROADBAND NETWORK	)	

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

PRELIMINARY AMENDMENT

Prior to the examination of the above continuation application, please amend this application as follows:

IN THE CLAIMS:

Please cancel claims 1-10 and 12-32.

Please add new claims 33-36 as follows:

-- 33. A method for representing a timing clock of a service input signal at a source node of a packet-based communications network including a network clock, the method comprising the steps of:

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defining a number of time intervals, each represented by a fixed number of timing clock cycles of the service input signal;

determining a number of network clock cycles respectively within each of the time intervals;

determining a modulo 2^P value of each of the determined number of network clock cycles, wherein 2^P represents a range of tolerance in the timing clock of the service input signal; and

transmitting each of the determined modulo 2^P values at the end of each of the time intervals respectively.

34. A method for representing a timing clock of a service input signal at a source node of a packet-based communications network including a network clock, the method comprising the steps of:

defining a number of time intervals each represented by a fixed number of timing clock cycles of the service input signal;

determining a number of network clock cycles respectively within each of the time intervals;

determining a modulo 2^P value of each of the determined number of network clock cycles, wherein 2^P represents a range of possible deviations in the

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number of network clock cycles within each of the time intervals; and

transmitting each of the determined modulo 2^P values at the end of each of the time intervals respectively.

35. A method for recovering a timing clock of a service input signal at a destination node of a packet-based communications network including a network clock, the method comprising, the steps of:

receiving a residual time stamp that represents a modulo 2^P value of a number of network clock cycles in a time interval defined by a fixed number of timing clock cycles of the service input signal, wherein 2^P represents a range of tolerance in the timing clock of the service input signal;

determining, from the residual time stamp and the network clock cycles, the time interval; and

recovering the timing clock of the service input signal based on the determined time interval and the fixed number of timing clock cycles.

36. A method for recovering a timing clock of a service input signal at a destination node of a packet-based communications network including a network clock, the method comprising the steps of:

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receiving a residual time stamp that represents a modulo 2^P value of a number of network clock cycles in a time interval defined by a fixed number of timing clock cycles of the service input signal, wherein 2^P represents a range of possible deviations in the number of network clock cycles within the time interval;

determining, from the residual time stamp and the network clock cycles, the time interval; and

recovering the timing clock of the service input signal based on the determined time interval and the fixed number of timing clock cycles.--

REMARKS

This Preliminary Amendment addresses issues raised in the Office Action dated December 30, 1998, in the parent application of this Rule 53(b) Continuation Application. In the Office Action, the Examiner rejected claims 34-37 under 35 U.S.C. §103(a) as being unpatentable over Ishikawa (JP 3-114333) in view of CCITT Study GroupXVIII/8 entitled "Proposed method to provide the clock recovery function for circuit emulation" (hereinafter "Matsuyama"). Claims 34-37 of the parent application appear in the present Continuation Application as new claims 33-36.

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Applicants have canceled claims 1-10 and 12-32, and added 33-36 claims to expedite prosecution of the parent application. Claim 11 has been retained for the purpose of filing this continuation reissue application. Claims 11 and 33-36 remain in the application.

Applicants respectfully disagree with the Examiner's rejections in the December 30, 1998 Office Action. On March 23, 1999, an interview was conducted with Examiner Vo to discuss the differences between the present invention and the references cited by the Examiner. At this interview Applicants agreed to provide a response, and Examiner Vo agreed to reconsider his rejections.

Ishiwaka, the primary reference cited by the Examiner discloses a clock synchronization format in which the transmitter transmits, in the form of packets, transmitter clock frequency data indicating the relative frequency of the transmitting clock. The receiver then compares a receiver clock frequency with the received transmitter clock frequency in order to synchronize the transmitter clock and receiver clock. Ishikawa does not address the question of how to transmit time stamp information like the present invention.

Matsuyama, the secondary reference relied on by the Examiner, does address time stamping, but merely discloses a time stamping technique in which reference

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timing is used to increment a modulo 2^{16} counter (16 bits) at the transmitter. This reference timing is derived from the either the timing of the physical interface or from the reception of a clock cell and is disclosed as the network reference timing. Every 16 cells the contents of this counter is read out and transferred to the receiver. This value is called the Time Stamp (TS), indicates the time this cell entered the ATM network, and requires a 16 bit cell to transmit the information.

In contrast, the present invention as recited in independent claims 33 and 35 recites determining or receiving a modulo 2^p value, wherein 2^p represents a range of tolerance in the timing clock of the service input. As described above, the 2^{16} counter disclosed in Matsuyama is used to determine the actual number of clock cycles during the time stamp period, and as such 2^{16} does not represent a range of tolerance in the timing clock.

As such, Matsuyama does not teach or suggest determining a modulo 2^p value, wherein 2^p represents a range of tolerance in the timing clock of the service input signal, as recited in new claims 33 and 35.

With regard to independent new claims 34 and 36, as described above, the 2^{16} counter disclosed in Matsuyama is used to determine the actual number of clock cycles during the time stamp period. In contrast, independent claims recite a determining a modulo 2^p value, wherein 2^p represents a range of possible deviations in the number of

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network clock cycles within each of the time intervals. Thus, the 2^{16} counter disclosed in Matsuyama does not represent a range of possible deviations in the number of clock cycles within each time interval, but instead represents the actual number of clock cycles in the time interval.

Accordingly, Applicants submit that neither Iwata nor Matsuyama taken alone or in combination, disclose or suggest the combination of elements as recited in claims 33-36.

For at least the foregoing reasons, Applicants submit that independent claims 33-36 are allowable over Iwata and Matsuyama.

Respectfully submitted,

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By: James K. Hammond
James K. Hammond
Reg. No. 31,964

Dated: April 16, 1999

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SYNCHRONOUS RESIDUAL TIME STAMP FOR

TIMING RECOVERY IN A BROADBAND NETWORK

BACKGROUND OF THE INVENTION

This invention relates to timing recovery of a source node service clock frequency at a destination node in a broadband asynchronous transfer mode (ATM) network where the source and destination nodes receive reference timing signals derived from a single master clock.

Asynchronous Transfer Mode (ATM) is a packet oriented technology for the realization of a Broadband Integrated Services Network (BISDN). By using ATM, network resources can be shared among multiple users. Moreover, various services including voice, video and data can be multiplexed, switched, and transported together under a universal format. Full integration will likely result in simpler and more efficient network and service administration and management. However, while conventional circuit-switching is optimized for real-time, continuous traffic, ATM is more suitable for the transport of bursty traffic such as data. Accommodation of constant bit rate (CBR) services is, however, an important feature of ATM, both for universal integration and for compatibility between existing and future networks. In the transport of a CBR signal through a broadband ATM network, the CBR signal is first segmented into 47-octet units and then mapped, along with an octet of ATM Type I Adaptation Layer (AAL) overhead, into the 48-octet payload of the cell. The

cells are then statistically multiplexed into the network and routed through the network via ATM switches.

It is essential to the proper delivery of such CBR service traffic in a broadband network that the clock controlling the destination node buffer be operating at a frequency precisely matched to that of the service signal input at the source node in order to avoid loss of information due to buffer over- or underflow. However, unlike the circuit-switched transport of service data wherein the clock frequency at the destination node may be traced directly back to that of the source node by the regular, periodic arrival of the CBR traffic, transport in an ATM network inherently results in cell jitter, i.e. the random delay and aperiodic arrival of cells at a destination node, which essentially destroys the value of cell arrival instances as a means for directly recovering the original service signal input frequency.

Such cell jitter, generally the result of multiplexing of transport cells in the broadband network and the cell queuing delays incurred at the ATM switches in the network, is substantially unpredictable. Thus, little is known about the cell arrival time beyond the fact that the average cell delay is a constant, assuming that the ATM network provides sufficient bandwidth to ensure against loss of cells within the network. As a means for closely approximating the service signal frequency at the destination node, some consideration had previously been given to utilizing a direct extension of circuit-switched timing recovery practices which rely entirely upon a buffer fill signal

as the basis for recovery of the source timing. However, due to the lack of knowledge of statistics of the cell jitter, this approach would have required a phase-locked loop with very low cut-off frequency (in the order of a few Hz) and would thus have resulted in excessive converging time and degradation of jitter and wander performance.

A number of schemes have been proposed to improve such a conventional manner of recovering service timing in the presence of cell jitter, yet none has achieved this end economically and without extensive control systems of notable complexity. Singh et al., for example, in "Adaptive Clock Synchronization Schemes For Real-Time Traffic In Broadband Packet Networks," 8th European Conference on Electrotechnics, Stockholm, Sweden, June 1988, and "Jitter And Clock Recovery For Periodic Traffic In Broadband Packet Networks," IEEE Globecom '88, Florida, December 1988, have proposed algorithms which attempt to more closely estimate cell jitter statistics and derive timing recovery from those indications. These adaptive approaches, suggested to be applicable to both synchronous and non-synchronous networks, rely upon the interaction of increasingly complex algorithms which would require the noted extensive controls for implementation.

These prior art schemes described above can be classified as non-synchronous techniques, which are based on the simple fact that the expected value of the network cell jitter is zero and thus rely on phase filtering. Synchronous techniques, on the other hand, utilize the fact that common timing is available at both the transmitter and the receiver. In a synchronous broadband

ATM network, such as the Synchronous Optical Network (SONET) prescribed by American National Standard, ANSI T1.105-1988, "Digital Hierarchy Optical Interface Rates and Formats Specification," 10 March 1988, the network source and destination node control clocks are synchronized to the same timing reference. As a result, there is no necessity for relying upon any extraneous phenomenon such as instants of cell arrival to provide a datum base for determining the relative frequencies of those control clocks. The effect of cell jitter caused by multiplexing and switching delays in the network is therefore of little consequence in any procedure for circuit transporting CBR service, which is based, as is the present invention, on an actual synchrony of node timing. Thus being devoid of concern for cell jitter, this process is free to simply determine the difference in frequency between the CBR service signal input at the source node and the source/destination node timing clock(s).

U.S. Patent No. 4,961,188 issued on October 2, 1990 to Chi-Leung Lau, co-inventor herein, discloses a synchronous frequency encoding technique (SFET) for clock timing in a broadband network. The SFET takes advantage of the common timing reference at both the source and the receiver. At the source, the asynchronous service clock is compared to the network reference clock. The discrepancy between properly chosen submultiples of the two clocks is measured in units of a preassigned number of slip cycles of network clock. This clock slip information is conveyed via a Frequency Encoded Number (FEN) which is carried in the ATM Adaptation Layer (AAL) overhead. At the receiver, the

common network clock and the FEN are used to reconstruct the service clock. This timing recovery process does not rely on any statistics of the cell jitter except that it has a known, bounded amplitude. Therefore, the recovered clock has jitter performance comparable to that of the circuit-switched network.

An alternative proposed approach is known as Time Stamp (TS). In the Time Stamp approach (see, for example, Gonzales et al, "Jitter Reduction in ATM Networks", Proceedings ICC'91, 9.4.1-9.4.6), the network clock is used to drive a multi-bit counter (16-bits in the proposal), which is sampled every fixed number of generated cells (e.g., 16). Thus, a fixed number, *N*, of service clocks cycles is used as the measuring yardstick. The sampled value of the 16-bit counter is the TS that inherently conveys the frequency difference information. Because of the size of the TS (2 octets), it has been proposed that the TS be transmitted via the Convergence Sublayer (CS) overhead. Thus the TS is a 16-bit binary number occurring once every *N* service clock cycles. Differences in successive TSs represent the quantized values of *M*, where *M* is the number of network clock cycles during the fixed TS period. At the receiver, the TS period is reconstructed from the received TSs and the network clock. A free-running 16-bit counter is clocked by the network clock and the output of the counter is compared to the received TSs which are stored in a TS FIFO. A pulse is generated whenever there is a match between the TS and the 16-bit counter. The service clock is recovered by supplying the resultant pulse stream as the reference signal to a multiply-by-*N* phase locked loop (PLL).

A comparison of the SFET approach and the TS approach reveals advantages and disadvantages for each. In the SFET approach there is a relatively stringent requirement on the derived network clock since it must be slightly larger than the service clock. Advantageously, however, a convergence sublayer is not required to transmit the FEN and only small overhead bandwidth is required to transmit the necessary information. On the other hand, the TS approach is more flexible in that it does not require stringent relationships between the service clock and the network derived clock and can therefore support a range of service bit rates. Disadvantageously, however, a rigid convergence sublayer structure is required to transmit the TS, which adds complexity and makes inefficient use of the overhead bandwidth.

An object of the present invention is to achieve synchronous timing recovery with an approach that has the advantages of both the SFET and TS approaches, specifically, the efficiency of SFET and the flexibility of TS.

SUMMARY OF THE INVENTION

As described hereinabove, the TS approach requires a large number of bits (16-bits in the example), to represent the number of network clock cycles within a time interval defined by a fixed number (N) of service clock cycles. In accordance with the present invention, the number of bits required to represent the number of network clock cycles within that time interval is substantially reduced. This is possible through the realization that the actual number of network clock cycles, M (where M is not necessarily an integer), deviates from a nominal known number of

cycles by a calculable deviation that is a function of *N*, the frequencies of the network and service clocks, and the tolerance of the service clock. Specifically, therefore, rather than transmitting a digital representation of the quantized actual number of network clock cycles within the interval, only a representation of that number as it exists within a defined window surrounding an expected, or nominal, number of network clock pulses is transmitted from a source node to a destination node in an ATM network. This representation will be referred to hereinafter as the Residual Time Stamp (RTS). By selecting the number of bits, *P*, so that all 2^P possible different bit patterns uniquely and unambiguously represent the range of possible numbers of network clock cycles within the fixed interval that is defined by *N* service clock cycles, the destination node can recover the service clock from the common network clock and the received RTS.

At the source node, a free-running *P*-bit counter counts clock cycles in a clock signal derived from the network clock. The service clock, which is derived from the incoming data signal to be transmitted over the ATM network, is divided by the factor of *N* to produce a pulse signal having a period (the RTS period) which defines the time interval for measuring the number (modulo 2^P) of derived network clock pulses. At the end of each RTS period, the current count of the free-running *P*-bit counter is sampled. That sampled value is the RTS, which is transmitted via the adaptation layer. Since the service clock from which the RTS period is defined and the derived network clock are neither synchronized nor integrally related in frequency, the actual number of derived

network clock cycles in a RTS period is unlikely to be an integer. Thus, when sampled at the end of each RTS period, the increment in the count of the *P*-bit counter is a quantized version of the count (modulo 2^P) of pulses in the RTS interval as modified by any accumulated fractional counts from a previous interval.

At the destination node, after the AAL is processed, the successive RTSs are converted into a pulse signal which has periods between pulses defined by the fixed integral numbers of derived network clock pulses that correspond to the conveyed RTS periods. Specifically, a free-running *P*-bit counter is driven by the derived network clock. A comparator compares this count with a stored received RTS and produces a pulse output upon a match. Since the count of the *P*-bit count matches the stored RTS every 2^P derived network clock cycles, comparator output pulses that do not actually present the end of the RTS period are inhibited by gating circuitry. This gating circuitry includes a second counter that counts the derived network clock cycles occurring since the end of the previous RTS period. When this second counter reaches a count equal to the minimum possible number of derived network clock pulses within an RTS period, the next comparator pulse output produced upon a match between the RTS and the count of the *P*-bit counter, is gated-through to the output and resets the second locked loop to recover the service clock.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 are timing diagrams showing the RTS concept of the present invention;

FIG. 2 is a block diagram showing apparatus, in accordance with the present invention, for generating the RTS at the source node of an ATM network;

FIG. 3 is a block diagram showing apparatus, in accordance with the present invention, for reconstructing the service clock at the destination node of an ATM network; and

FIG. 4 are timing diagrams showing the gating function at the apparatus of FIG. 3.

DETAILED DESCRIPTION

The concept of the Residual Time Stamp is described with reference to FIG. 1. In FIG. 1, and in the description hereinafter, the following terminology is used:

f_n ---- network clock frequency e.g. 155.52 MHz;

f_{nx} ---- derived network clock frequency, $f_{nx} = \frac{f_n}{x}$, where x is a rational number;

f_s ---- service clock frequency;

N ---- period of RTS in units of the service clock (f_s) cycles;

T_n ---- the n-th period of the RTS in seconds;

$\pm\varepsilon$ ---- tolerance of the source clock frequency in parts per million;

M_n (M_{nom}, M_{max}, M_{min}) ---- number of f_{nx} cycles within the *n-th* (nominal, maximum, minimum) RTS period, which are, in general, non-integers.

As can be noted in FIG. 1, during the *n-th* period, T_n, corresponding to N service clock cycles, there are M_n network

derived cycles. As aforenoted, since the service clock and the network clock are neither synchronized nor integrally related in frequency, this number of derived network clock cycles is not an integer. Since all practical timing recovery techniques transmit only integer values, the fractional part of M_n must be dealt with. Simple truncation or rounding of the fractional part in each RTS time slot is not permissible, as this would lead to a "random walk" type error accumulation. Rather, it is necessary to accumulate the fractional parts at the transmitter and use the accumulated value to modify the transmitted integer quantity. Since it is most convenient to generate RTS by an asynchronous counter, as will be described hereinafter in conjunction with the description of FIG. 2, a "truncation" operation is natural, reflecting the fact that an asynchronous counter's output does not change until the subsequent input pulse arrives. To formalize these notions, S_n is defined as the truncated value of M_n after accounting for the left over fractional part, d_n, from the (n-1)-th interval, viz.,

$$S_n = [M_n + d_n] \tag{1}$$

and

$$d_{n+1} = d_n + M_n - S_n \tag{2}$$

where [a] denotes the largest integer less than or equal to a. Since for accurate clocks, the range of M_n is very tightly constrained, i.e., $M_{max} - M_{min} = 2y << M_n$, the variation in S_n is also much smaller than its magnitude. It follows from Equation

(1) that

$$[M_{min} + d_n] \leq S_n \leq [M_{max} + d_n] \quad (3)$$

Since the maximum and minimum of d_n are 1 and 0 respectively, S_n is bounded by,

$$[M_{min}] \leq S_n \leq [M_{max}] + 1 \quad (4)$$

This implies, that the most significant portion of S_n carries no information and it is necessary to transmit only its least significant portion. This, therefore, is the essential concept of the RTS. The minimum resolution required to represent the residual part of S_n unambiguously is a function of N, the ratio of the network derived frequency to the service frequency, and the service clock tolerance, $\pm\varepsilon$. The maximum deviation, y, between the nominal number of derived network clock pulses in an RTS period, M_{nom}, and the maximum or minimum values of M (M_{max} or M_{min}) is given by,

$$y = N \times \frac{f_{nx}}{f_s} \times \varepsilon \quad (5)$$

where M_{nom} equals $N \times \frac{f_{nx}}{f_s}$

A specific numerical example can be considered for clarity of understanding. As illustrative derived network clock frequency and service clock frequencies could be given by f_{nx} = 155.52 MHz (for x=1), and f_s=78.16 MHz (nominal), respectively. A typical RTS sampling period (N) is 3008, which corresponds to a period of 8 cells and a 47-octet payload per cell (47 bytes/cell x 8 bits/ byte x 8 cells per RTS period). Using these numbers,

M_{nom}=5985.2119. If it is further reasonable to assume that the service clock tolerance is 200 parts per million, i.e., $\pm 200\text{x}10^{-6}$. From equation (5), therefore, y=1.197, which demonstrates that it is superfluous to transmit the full S_n in each RTS sampling period and transmission of the last few (P) bits of S_n is sufficient. This P-bit sample is the Residual-TS (RTS).

FIG. 2 is a block diagram of the source node of an ATM network showing apparatus for generating and transmitting the RTS. The basic network clock, C, shown at 10, serves as the reference for timing of all nodes of the synchronous network being here considered. This clock, having a frequency f_n, is divided in frequency by a rational factor x by a divider 11 to produce a derived network clock having a frequency f_{nx}. Preferably, x would be an integer value. The dividing factor is chosen so that the P bits available can unambiguously represent the number of derived network clock cycles within an RTS period. In the case where $\frac{f_{nx}}{f_s}$ is less than or equal to two, as in the example above, it can be shown that a 3-bit RTS is sufficient.

The derived network clock, f_{nx}, drives a P-bit counter, which is continuously counting these derived network clock pulses, modulo 2^P. The service clock, f_s, on lead 13, which is derived from the service data signal (not shown) to be transmitted over the ATM network, is divided in frequency by N, the desired RTS period in units of f_s cycles, by divide-by N circuit 14. As shown in FIG. 2, the output of divider 14 is a pulse signal in which T_n is its n-th period. At every T seconds (N source clock cycles)

latch 15 samples the current count of counter 12, which is then the P-bit RTS to be transmitted. As aforedescribed, this number represents the residual part of S_n and is all that is necessary to be transmitted to recover the source clock at the destination node of the network.

Each successive RTS is incorporated within the ATM adaptation layer overhead by AAL processor 16. The associated data to be transmitted (not shown) is also processed by processor 16 to form the payload of the cells, which are then assembled by an ATM assembler 17, which adds an ATM header for transmission over the network 18.

With reference again to the previous example, a four-bit counter (P=4) can be assumed to be used. Since M_{nom}=5985.2119 and 5985.2119 (modulo 16)=1.2119, a typical RTS output sequence when the source is at nominal frequency will be as follows;

....5,6,7,9,10,11,12,13,15,1,2,...

Since the counter 16, in effect, quantizes by truncation, the RTS changes only by integer values. The changes in RTS are such that their average is exactly equal to M_{nom} (modulo 2^P). In this example, the changes are either 1 or 2 with the change of 2 occurring either every 4 or 5 RTSs in such a way that the average interval is 1/0.2119-4.7198. In general, successive RTSs are related by

$$RTS_{n+1}=RTS_n + S_n = RTS_n + [d_n + M_n] \text{ (modulo } 2^P) \qquad (6)$$

In order to guarantee that no information is lost due to the modulo arithmetic, i.e., that the transmitted RTS represents S_n

unambiguously, it can be seen from equation (4) that the number of bits used for transmission must satisfy:

$$2^{P} \geq [M_{max}] - [M_{min}] + 2 \qquad (7)$$

Thus, in the example above, the number of bits allocated to the RTS must be 3 or greater. It can be noted that the number of bits necessary to unambiguously represent the number of derived network clock cycles within the RTS period is substantially less than the number of bits that would be required to represent the absolute number of clock cycles within the same interval. In the example above, for example, a 13-bit number would be required to represent M_{nom}.

If equation (7) is satisfied, knowledge of M_{nom} in the receiver at the destination node along with the received RTSs can be used to reproduce the service clock from the synchronous network clock. FIG. 3 shows one receiver implementation for reproducing the service clock from the received RTSs. At the receiver the common network clock 10 is available as it was at the transmitter. As in the transmitter, a divider 31 divides the network clock frequency, f_n by the same factor of x as divider 11 in the source node, to produce the same derived network clock signal having a frequency f_{nx} as was used by the transmitter at the source node of FIG. 2.

In a structure paralleling the transmitter in FIG. 2, a disassembler 32 processes the ATM headers received from the network 18 and passes the payload to an AAL processor 33. In addition to extracting the transmitted data (not shown), processor 33 extracts the periodic transmitted RTSs, which are sequentially

stored in a FIFO 34, which is used to absorb the network cell jitter. The earliest received RTS in FIFO 34 is compared by P-bit comparator 35 with the count of a free running P-bit counter 36, driven by the derived network clock f_{nx}. Whenever the output of counter 36 matches the current RTS, comparator 35 generates a pulse. Since counter 36 is a modulo 2^P counter, the RTS in FIFO 34 matches the count of counter 36 every 2^P derived network clock pulses, f_{nx}. The output of comparator 35 thus consists of a train of pulses that are separated, except for the first pulse, by 2^P cycles of the derived network clock. In order to select the output pulse of comparator 35 that corresponds to the end of the fixed period of the transmitted service clocks, which is the period per RTS to be recovered, gating circuitry 37 is employed. Gating circuitry 37, which includes a counter 38, a gating signal generator 39, and an AND gate 40, gates only that pulse output of comparator 35 produced after counting, from the last gated output pulse, a minimum number, M_1, of derived network clock cycles. This minimum number, M_1, is given by:

$$M_1 = [M_{nom}] - 2^{(P-1)} \qquad (8)$$

This ensures that $[M_{max}] - 2^P < M_1 < [M_{min}]$, and thus the gating pulse is guaranteed to select the correct RTS.

The gating function is best explained in conjunction with the timing diagrams of FIG. 4. Initially, it can be assumed that gating signal generator 39 is set to keep AND gate 40 open. Comparator 35 compares the first RTS in FIFO 34 with the free-running count of counter 36. When the count of counter 36 matches this first RTS, shown in FIG. 4 as "2", comparator 35 produces a

pulse which is gated through AND gate 40. This gated output pulse resets gating signal generator 39 thereupon turning off AND gate 40, resets the counter of counter 38 to zero, and reads the next stored RTS, "5", in FIFO 34. When counter 36 reaches the count of "5", comparator 35 produces another output pulse. AND gate 40, however, is OFF and remains off until counter 38 counts M_1 derived network clock cycles. Therefore, as noted in FIG. 4, all the subsequent matches of the RTS, "5" and the count of counter 36, which occur every 2^P derived network clock cycles, are blocked by AND gate 40. These subsequent pulses are blocked until counter 38 reaches a count of that minimum number of clock cycles that can comprise the fixed interval to be recovered from the RTS. After counting M_1 derived network clock cycles, counter 38 generates a pulse which signals gating signal generator 39 to open AND gate 40. The next pulse produced by comparator 35 upon the match between the RTS in FIFO 34 and the count of counter 36 is gated through AND gate 40. This pulse, as before, resets counter 38, resets gating signal generator 39, and reads-in the next stored RTS to the output of FIFO 34. The resultant time difference between output pulses of AND gate 40 is the desired fixed time interval, S_n, to be recovered from the transmitted RTSs. As previously defined in equation (1), S_n is the truncated value in the nth interval, after accounting for a left over portion from the (n-1)-th interval, of the actual number of derived network clock cycles within the fixed interval defined by N source clock cycles. As can be noted, S_n modulo (2^P) is equal to the difference of the RTSs associated with the pulses matched by

comparator 35 right before and right after the reset. Thus in FIG. 4, for the n-th period, this is the difference between "5" and "2", or "3", and for the (n+1)-st period, this is the difference between "9" and "5" or "4". The resultant pulse train at the output of gating circuitry 37 can be seen to duplicate the signal at the source node of the network, which is defined by *N* service clock cycles, as modified by the quantization effect of the RTSs. This pulse stream is input to a multiply-by *N* phase-locked loop 41 which multiplies the frequency by the factor of *N* and smooths out the variation of the reproduced periods. The resultant output clock signal, f_r, is the reproduced service timing signal, which can be employed by the circuitry at the destination node.

The above-described embodiment is illustrative of the principles of the present invention. Other embodiments could be devised by those skilled in the art without departing from the spirit and scope of the present invention.

WHAT IS CLAIMED IS:

1. A method of recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said packet-based telecommunications network, the destination node and the source node having a common network clock, comprising the steps of:

(a) at the source node, dividing the timing clock of the service input by a factor of an integer N to form residual time stamp (RTS) periods;

(b) at the source node, counting the network clock cycles modulo 2^P, where 2^P is less than the number of network clock cycles within an RTS period and P is chosen so that the 2^P counts uniquely and unambiguously represent the range of possible network clock cycles within an RTS period;

(c) transmitting from the source node to the destination node an RTS at the end of each RTS period that is equal to the modulo 2^P count of network clock cycles at that time;

(d) determining from the RTSs received at the destination node, the number of network clock cycles in each RTS period;

(e) generating a pulse signal from the network clock at the destination node in which the period between each pulse in the pulse signal equals the determined number of network clock cycles in the corresponding RTS period; and

(f) multiplying the frequency of the pulse signal generated in step (e) by the same factor of an integer N used in step (a) to recover the timing clock of the service input.

2. The method of claim 1 wherein the network clock frequency is less than or equal to twice the service clock frequency.

3. A method of recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said packet-based telecommunications network, the destination node and the source node having a common network clock, comprising the steps of:

(a) at the source node, dividing the timing clock of the service input by a factor of an integer N to form residual time stamp (RTS) periods;

(b) at the source node, dividing the network clock by a rational factor to form a derived network clock;

(c) at the source node, counting the derived network clock cycles modulo 2^P, where 2^P is less than the number of derived network clock cycles within an RTS period and P is chosen so that the 2^P counts uniquely and unambiguously represent the range of possible derived network clock cycles within an RTS period;

(d) transmitting from the source node to the destination node an RTS at the end of each RTS period that is equal to the modulo 2^P count of derived network clock cycles at that time;

(e) at the destination node dividing the network clock by the same rational factor used at the source node to form a derived network clock equal to the derived network clock at the source node;

(f) determining from the RTSs received at the destination node, the number of derived network clock cycles in each RTS period;

(g) generating a pulse signal from the derived network clock at the destination node in which the period between each pulse in the pulse signal equals the determined number of derived network clock cycles in the corresponding RTS period; and

(h) multiplying the frequency of the pulse signal generated in step (g) by the same factor of an integer N used in step (a) to recover the timing clock of the service input.

4. The method of claim 3 wherein the derived network clock frequency is less than or equal to twice the service clock frequency.

5. Apparatus for recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said packet-based telecommunications network, the destination node and the source node having a common network clock, comprising at the source node:

dividing means for dividing the timing clock of the service input by a factor of an integer N to form residual time stamp (RTS) periods;

counting means connected to the network clock for counting network clock cycles modulo 2^P, where 2^P is less than the number of network clock cycles within an RTS period and P is chosen so that the 2^P counts uniquely and unambiguously represent the range of possible network clock cycles within an RTS period; and

transmitting means, responsive to the RTS periods formed by said dividing means and the count of said counting means, for transmitting over the telecommunications network an RTS at the end of each RTS period that is equal to the modulo 2^{p} count of network clock cycles at that time;

and comprising at the destination node:

receiving means for receiving the RTSs transmitted over the telecommunications network by said transmitting means;

converting means responsive to the received RTSs and the network clock for converting the received RTSs into a pulse signal in which the periods between pulses are determined from the numbers of network clock cycles associated with the counts of network clock cycles within said RTS periods; and

means for multiplying the frequency of the pulse signal generated by said converting means by the same factor of an integer N used in said dividing means for recovering the timing clock of the service input.

6. Apparatus in accordance with claim 5 wherein the network clock frequency is less than or equal to twice the service clock frequency.

7. Apparatus in accordance with claim 5 wherein said converting means comprises:

means for sequentially storing the received RTSs;

means for counting network clock cycles modulo 2^{p};

comparing means for comparing the modulo 2^{p} count of network clock cycles with a stored RTS and for generating a pulse each time the count of network clock cycles matches the RTS; and

gating means for gating to said multiplying means, for each sequentially received and stored RTS, the pulse produced by said comparing means that occurs after the counting means counts, starting-in-time from the previous gated pulse, a number of network clock cycles that is greater than a predetermined minimum absolute number of network clock cycles that can occur within any RTS period.

8. Apparatus for recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said packet-based telecommunications network, the destination node and the source node having a common network clock, comprising at the source node:

first dividing means for dividing the timing clock of the service input by a factor of an integer N to form residual time stamp (RTS) periods;

second dividing means for dividing the network clock by a rational factor to form a derived network clock;

counting means connected to the network clock for counting derived network clock cycles modulo 2^P, where 2^P is less than the number of derived network clock cycles within an RTS period and P is chosen so that the 2^P counts uniquely and unambiguously represent the range of possible derived network clock cycles within an RTS period; and

transmitting means, responsive to the RTS periods formed by said first dividing means and the count of said counting means, for transmitting over the telecommunications network an RTS at the

end of each RTS period that is equal to the modulo 2^P count of derived network clock cycles at that time;

and comprising at the destination node:

receiving means for receiving the RTSs transmitted over the telecommunications network by said transmitting means;

means for dividing the network clock by the same rational factor used at the source node to form a derived network clock;

converting means responsive to the received RTSs and the derived network clock for converting the received RTSs into a pulse signal in which the periods between pulses are determined from the numbers of derived network clock cycles associated with the counts of derived network clock cycles within said RTS periods; and

means for multiplying the frequency of the pulse signal generated by said converting means by the same factor of an integer N used in said first dividing means for recovering the timing clock of the service input.

9. Apparatus in accordance with claim 8 wherein the derived network clock frequency is less than or equal to twice service clock frequency.

10. Apparatus in accordance with claim 8 wherein said converting means comprises:

means for sequentially storing the received RTSs;

means for counting derived network clock cycles modulo 2^P;

comparing means for comparing the modulo 2^P count of derived network clock cycles with a stored RTS and for generating a pulse each time the count of derived network clock cycles matches the RTS; and

gating means for gating to said multiplying means, for each sequentially received and stored RTS, the pulse produced by said comparing means that occurs after the counting means counts, starting-in-time from the previous gated pulse, a number of derived network clock cycles that is greater than a predetermined minimum absolute number of derived network clock cycles that can occur within any RTS period.

11. Apparatus for generating a representation of the relationship between the timing clock of a service input, at a source node of a packet-based telecommunications network, and a network clock, the apparatus comprising:

(a) means, at the source node, defining a residual time stamp (RTS) period as an integral number N of source-node service clock cycles;

(b) means, at the source node, defining a derived network clock frequency f_{nx} from a network frequency f_n where $f_{nx} = f_n/x$ is a rational number, and f_{nx} is less than or equal to twice the service clock frequency;

(c) means, at the source node, for counting the derived network clock cycles modulo 16 in an RTS period and;

(d) means for transmitting from the source node an RTS that is equal to the modulo 16 count of derived network clock cycles in the RTS period.

12. Apparatus for recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of the packet-based telecommunications network, wherein the destination and source nodes have a common network clock or divided network clock and wherein the service node generates a residual time stamp (RTS) signal equal to a modulo 16 count of cycles based on the network clock; the apparatus comprising:

means for receiving the RTS signal;

means for determining the number of network cycles in an RTS period from the RTS signal; and

means responsive to the determining means for generating a clock signal which represents a recovery of the timing clock of the service input.

13. Apparatus for generating a representation of a timing clock of a service input at a source node of a packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the source node and a destination node; the apparatus comprising:

(a) means for defining a time interval by a fixed number of service clock cycles; and

(b) means for generating a digital representation of a variance of a quantized actual number of network clock cycles within the time interval from an expected number of network clock cycles within the time interval, the variance being within a defined time window which corresponds to a frequency variation of

the source-node service clock and which surrounds the expected number of network clock cycles.

14. The apparatus of claim 13, wherein the digital representation represents a chosen number of the least significant bits of the quantized actual number, the chosen number being sufficient to represent a range of variances based on the source-node service clock variation.

15. The apparatus of claim 14 wherein the chosen number is 4.

16. Apparatus for recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said network, wherein a common network clock or divided network clock is provided for the destination node and the source node and a time interval is defined by a fixed number of source-node service clock cycles; the apparatus comprising:

means for receiving a digital representation of a variance of a quantized actual number of network clock cycles from a nominal number of network clock cycles within the time interval, the variance being within a defined time window which corresponds to a source-node service clock variation and which surrounds the nominal number of network clock cycles; and

means for recovering the source-node service clock at the destination node by constructing a timing signal at the destination node based on the variance.

17. Apparatus for reconstructing, at a destination node of a packet-based telecommunications network, a timing clock of a

service input at a source node of the network, wherein a common network clock or divided network clock is provided for the destination node and the source node and wherein the reconstruction is based on successive modulo 2^P numerical representations of the number of network clock cycles within corresponding predetermined time periods, each of the numerical representations being received from the source node and being less than the actual number of network clock cycles within its corresponding time period; the apparatus comprising:

means for receiving the numerical representations in succession at the destination node;

means for converting the received numerical representations into successive fixed time intervals, wherein each successive interval corresponds to the number of network clock cycles in a corresponding one of the predetermined time periods; and

means for recovering the source-node service clock from the fixed time intervals.

18. The apparatus of claim 17, wherein the converting means further comprises:

means for sequentially storing the successive modulo 2^P numerical representations;

means for comparing the successive numerical representations with a modulo 2^P count of the network clock cycles at the destination node to generate a comparison signal for each match between the numerical representation and the modulo 2^P count at the destination node; and

means for successively selecting from the comparison signal the numerical representations occurring after a predetermined minimum number of network clock cycles which can occur within any of the predetermined time periods, wherein the successive selected numerical representations define the successive fixed time intervals.

19. A method for generating a signal at a source node for use in recovering a source-node service clock at a destination node in a packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the source and destination nodes; the steps of the method comprising:

defining a time interval by a fixed number of cycles of the source-node service clock;

determining an actual number of cycles of the network clock within the time interval;

determining a numerical deviation of the actual number of network clock cycles from another number of network clock cycles known nominally to be within the time interval; and

generating a digital signal representing the numerical deviation for transmission through the network to the destination node.

20. A method for recovering a source-node service clock at a destination node in a packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the source and destination nodes, wherein a time interval is defined by a fixed number of cycles of the source-node service clock, and wherein an actual number of cycles of the

network clock within the time interval and a numerical deviation of the actual number of network clock cycles from another number of network clock cycles known nominally to be within the time interval are determined; the steps of the method comprising:

receiving a digital signal representing the numerical deviation transmitted through the network from the source node; and

generating a timing signal corresponding to the source-node service clock on the basis of the digital signal representing the numerical deviation.

21. A method for recovering, at a destination node of a packet-based telecommunications network, a timing clock of a service input at a source node of the packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the destination node and the source node; the steps of the method comprising:

defining a time interval by a fixed number of cycles of the source-node service clock;

determining an actual number of cycles of the network clock within the time interval;

determining a numerical deviation of the actual number of network clock cycles from another number of network clock cycles known nominally to be within the time interval;

generating a digital signal representing the numerical deviation;

transmitting the digital signal to the destination node; and

generating a timing signal at the destination node corresponding to the source node service clock on the basis of the digital signal and a signal from the network clock.

22. The method of claim 21 wherein the numerical deviation is determined as a function of the fixed number of source-node service clock cycles, the frequencies of the network clock and the source-node service clock, and a frequency variation of the source-node service clock.

23. The method of claim 21 further including the step of employing a modulo 2^P counter to generate the numerical deviation.

24. Apparatus for generating a signal at a source node for use in recovering a source-node service clock at a destination node in a packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the source and destination nodes; the apparatus comprising:

means for defining a time interval by a fixed number of cycles of the source-node service clock;

means for determining an actual number of cycles of the network clock within the time interval;

means for determining a numerical deviation of the actual number of network clock cycles from another number of network clock cycles known nominally to be within the time interval; and

means for generating a digital signal representing the numerical deviation for transmission through the network to the destination node.

25. The apparatus of claim 24 wherein the numerical deviation is determined as a function of the fixed number of

source-node service clock cycles, the frequencies of the network clock and the source-node service clock, and a frequency variation of the source-node service clock.

26. The apparatus of claim 24 wherein the numerical deviation determining means includes a modulo 2^P counter which generates the numerical deviation.

27. The apparatus of claim 26 wherein a value of 2^P is 16.

28. Apparatus for recovering a source-node clock at a destination node in a packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the source and destination nodes and wherein a time interval is defined by a fixed number of cycles of the source-node service clock, and wherein an actual number of cycles of the network clock within the time interval and a numerical deviation of the actual number of network clock cycles from another number of network clock cycles known nominally to be within the time interval are determined; the apparatus comprising:

means for receiving a digital signal representing the numerical deviation transmitted through the network from the source node; and

means for generating a timing signal corresponding to the source-node service clock on the basis of the digital signal representing the numerical deviation.

29. Apparatus for recovering, at a destination node of a packet-based telecommunications network, a timing clock of a service input at a source node of the packet-based telecommunications network, wherein a common network clock or

divided network clock is provided for the destination node and the source node; the apparatus comprising:

means for defining a time interval by a fixed number of cycles of the source-node service clock;

means for determining an actual number of cycles of the network clock within the time interval;

means for determining a numerical deviation of the actual number of network clock cycles from another number of network clock cycles known nominally to be within the time interval;

means for generating a digital signal representing the numerical deviation;

means for transmitting the digital signal to the destination node; and

means for generating a timing signal at the destination node corresponding to the source-node service clock on the basis of the digital signal and a signal from the network clock.

30. The apparatus of claim 29 wherein the numerical deviation is determined as a function of the fixed number of source-node service clock cycles, the frequencies of the network clock and the source-node service clock, and a frequency variation of the source-node service clock.

31. The apparatus of claim 29 wherein the numerical deviation determining means includes a modulo 2^P counter which generates the numerical deviation.

32. The apparatus of claim 29 wherein means are provided for carrying any fractional network cycle in any time interval for

<u>network cycle counting by the modulo 2^P counter for counting the next time interval.</u>

ABSTRACT

A Residual Time Stamp (RTS) technique provides a method and apparatus for recovering the timing signal of a constant bit rate input service signal at the destination node of a synchronous ATM telecommunication network. At the source node, a free-running P-bit counter counts cycles in a common network clock. At the end of every RTS period formed by N service clock cycles, the current count of the P-bit counter, defined as the RTS, is transmitted in the ATM adaptation layer. Since the absolute number of network clock cycles likely to fall within an RTS period will fall within a range determined by N, the frequencies of the network and service clocks, and the tolerance of the service clock, P is chosen so that the 2^P possible counts, rather than representing the absolute number of network clock cycles and RTS period, provide sufficient information for unambiguously representing the number of network clock cycles within that predetermined range. At the destination code, a pulse signal is derived in which the periods are determined by the number of network clock cycles represented by the received RTSs. This pulse signal is then multiplied in frequency by N to recover the source node service clock.

PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of:

U.S. Patent No. 5,260,978

Patentees: Paul E. Fleischer et al.

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For: SYNCHRONOUS RESIDUAL TIME STAMP FOR TIMING RECOVERY IN A BROADBAND NETWORK

Group Art Unit: 2614

Examiner: Hai H. Phan

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

REISSUE DECLARATION UNDER 37 C.F.R. § 1.175

I, Paul E. Fleischer hereby declare:

1. I am an original, first, and one of the named joint inventors, along with named joint inventor Chi-Leung Lau, of the invention disclosed and claimed in the attached specification, entitled SYNCHRONOUS RESIDUAL TIME STAMP FOR TIMING RECOVERY IN A BROADBAND NETWORK, for U.S. Patent 5,260,978 (hereinafter, "the '978 patent"), which was filed on October 30, 1992 and issued on November 9, 1993, for which a reissue application is sought. I have reviewed and understand the contents of the attached specification, including the claims.

2. I have a residence, a post office address, and citizenship as indicated below next to my name.

3. I believe that the '978 patent is partly inoperative because the patent claims embrace less than we had a right to claim, by being too narrow in at least some aspects, and thus erroneously fail to protect all important aspects of the invention disclosed in the '978 patent. I believe that these claim errors arose as a result of a combination of my lack of expertise in the legal interpretation of claims and my reliance on the original working attorney to appreciate the full scope of the invention.

4. I understand that the new claims in this reissue application are broadened in certain aspects to correct such inoperativeness, while maintaining the original claims without change so as to obtain the scope of the new broadened claims while retaining the scope of the original claims.

5. The claiming errors, generally referenced in ¶ 3 and specifically identified in ¶ 9, occurred without any deceptive intention on my part.

6. I acknowledge my duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in 37 C.F.R. § 1.56.

7. I first learned of claiming errors, which make the '978 patent partly inoperative, in October-November 1995 in response to a request that I review the patent.

8. In supporting the preparation of the application for the '978 patent, I recollect having read the description in the

specification, for technical accuracy and completeness of the disclosure and having reviewed the claims as filed for the '978 patent. I recollect having made suggestions for the claims, but ultimately relied on the judgment of the working attorney in the choice of claim language which would properly define the metes and bounds of the invention.

9. The following are specifically identified as claiming errors:

A. All of the original '978 patent claims are directed to a packet-based telecommunications network as a whole.

I believe broadened claims for the invention as applied either at a sending node or a destination node are justified by the invention of the '978 patent.

New claims 11, 13-15, 19, and 24-27 are broadened to recite only a source node apparatus or method. New claims 12, 16-18, 20, and 28 are broadened to recite only a destination node apparatus or method.

B. None of the original '978 patent claims are broadly directed to the invention apparatus and/or method in correspondence to broad aspects of the text in the Summary of the Invention of the '978 patent.

The invention is summarized, in part, in column 3, lines 52-67 of the original '978 patent, as follows:

> In accordance with the present invention, the number of bits required to represent the number of network clock cycles within that time interval is substantially reduced. This is possible through the realization that the actual number of network clock cycles, M (where M is not necessarily an integer), deviates from a nominal known number of cycles

by a calculable deviation that is a function of N, the frequencies of the network and service clocks, and the tolerance of the service clock. Specifically, therefore, rather than transmitting a digital representation of the quantized actual number of network clock cycles within the interval, only a representation of that number as it exists within a defined window surrounding an expected, or nominal, number of network clock pulses is transmitted from a source node to a destination node in an ATM network.

New network combination claims 21-23 and 29-32 and the new sending node and destination node claims 16-20 and 24-28 are broadened to recite broad aspects of the invention as described in the text of the Summary of the Invention. Claims 16-18 include a quantized difference within a defined time window. Claims 19-32 include, in apparatus or method format, a deviation of determined network clock cycles (in a defined time interval) from a nominal number of network clock cycles for the time interval.

C. None of the original '978 patent claims recite a specific numeric value for the modular counting or the feature of carryover of any fraction in the modulo count in any one counting period to the next counting period.

New independent claims 11, 14, and dependent claim 27, while broadened in other aspects, recite or correspond to a modular counting value of 16. New claim 32 depends from broadened claim 29 and recites the carryover feature.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false

statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint Leonard Charles Suchyta (Reg. No. 25,707) my attorney, with full power of substitution and revocation, to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected therewith.

It is respectfully requested that all written communications from the Patent and Trademark Office in connection with this application be addressed to Leonard Charles Suchyta, Bell Communications Research, Inc., Morris Corporate Center, 445 South Street, Morristown, New Jersey 07960-6438.

Dated: Nov 7, 1995

Paul E. Fleischer

PATENT
BOX REISSUE
Attorney Docket No.: 1333-0116

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of:

U.S. Patent No. 5,260,978

Patentees: Paul E. Fleischer et al.

Issued: November 9, 1993

Serial No.: 07/969,592

Filed: October 30, 1992

For: SYNCHRONOUS RESIDUAL TIME STAMP FOR TIMING RECOVERY IN A BROADBAND NETWORK

Group Art Unit: 2614

Examiner: Hai H. Phan

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

REISSUE DECLARATION UNDER 37 C.F.R. § 1.175

I, Chi-Leung Lau hereby declare:

1. I am an original, first, and one of the named joint inventors, along with named joint inventor Paul E. Fleischer of the invention disclosed and claimed in the attached specification, entitled SYNCHRONOUS RESIDUAL TIME STAMP FOR TIMING RECOVERY IN A BROADBAND NETWORK, for U.S. Patent 5,260,978 (hereinafter, "the '978 patent"), which was filed on October 30, 1992 and issued on November 9, 1993, for which a reissue application is sought. I have reviewed and understand the contents of the attached specification, including the claims.

2. I have a residence, a post office address, and citizenship as indicated below next to my name.

3. I believe that the '978 patent is partly inoperative because the patent claims embrace less than we had a right to claim, by being too narrow in at least some aspects, and thus erroneously fail to protect all important aspects of the invention disclosed in the '978 patent. I believe that these claim errors arose as a result of a combination of my lack of expertise in the legal interpretation of claims and my reliance on the original working attorney to appreciate the full scope of the invention.

4. I believe that the new claims in this reissue application are broadened in certain aspects to correct such inoperativeness, while maintaining the original claims without change so as to obtain the scope of the new broadened claims while retaining the scope of the original claims.

5. The claiming errors, generally referenced in ¶ 3 and specifically identified in ¶ 9 occurred without any deceptive intention on my part.

6. I acknowledge my duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in 37 C.F.R. § 1.56.

7. I first learned of claiming errors, which make the '978 patent partly inoperative, in October-November 1995 in response to a request that I review the patent.

8. Since I have no legal expertise, I principally supported preparation of the application for the '978 patent by

reviewing the description in the specification for general clarity, technical accuracy, and completeness of the disclosure. I reviewed the claims as filed for the '978 patent primarily with reliance on the working attorney in the choice of claim language which would properly define the invention.

9. The following are specifically identified as claiming errors:

A. All of the original '978 patent claims are directed to a packet-based telecommunications network as a whole.

I believe broadened claims for the invention as applied either at a sending node or a destination node are justified by the invention of the '978 patent.

New claims 11, 13-15, 19, and 24-27 are broadened to recite only a source node apparatus or method. New claims 12, 16-18, 20, and 28 are broadened to recite only a destination node apparatus or method.

B. None of the original '978 patent claims are broadly directed to the invention apparatus and/or method in correspondence to broad aspects of the text in the Summary of the Invention of the '978 patent.

The invention is summarized, in part, in column 3, lines 52-67 of the original '978 patent, as follows:

> In accordance with the present invention, the number of bits required to represent the number of network clock cycles within that time interval is substantially reduced. This is possible through the realization that the actual number of network clock cycles, M (where M is not necessarily an integer), deviates from a nominal known number of cycles by a calculable deviation that is a function of N, the frequencies of the network and

> service clocks, and the tolerance of the service clock. Specifically, therefore, rather than transmitting a digital representation of the quantized actual number of network clock cycles within the interval, only a representation of that number as it exists within a defined window surrounding an expected, or nominal, number of network clock pulses is transmitted from a source node to a destination node in an ATM network.

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imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint Leonard Charles Suchyta (Reg. No. 25,707) my attorney, with full power of substitution and revocation, to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected therewith.

It is respectfully requested that all written communications from the Patent and Trademark Office in connection with this application be addressed to Leonard Charles Suchyta, Bell Communications Research, Inc., Morris Corporate Center, 445 South Street, Morristown, New Jersey 07960-6438.

Dated: Nov. 7, 1995.

Chi-Leung Lau

FIG. 1

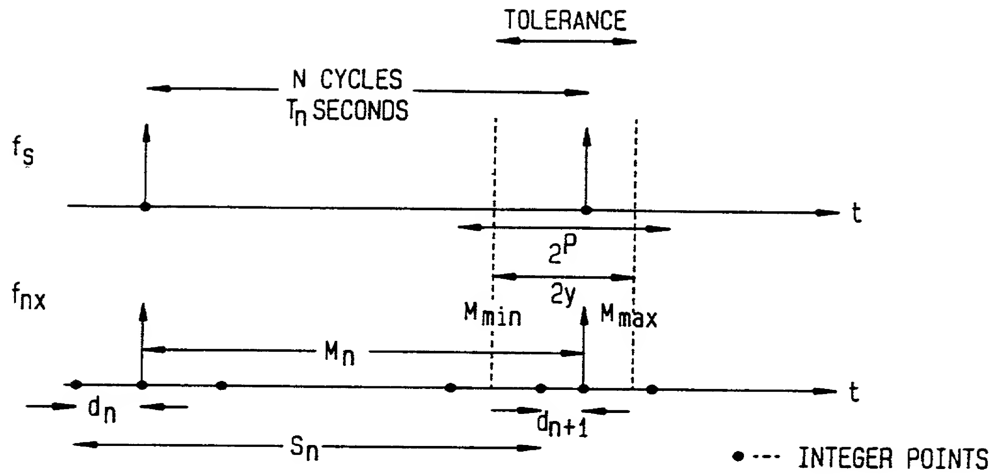
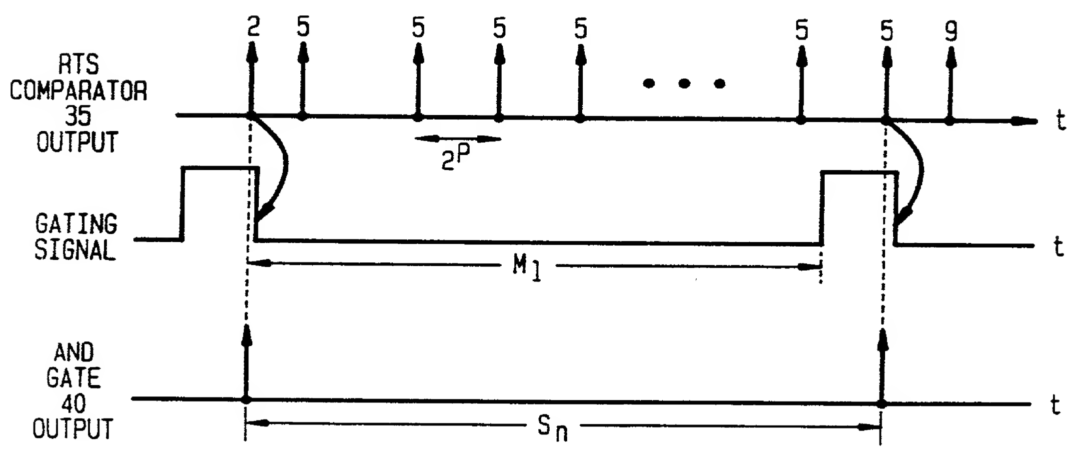

TOLERANCE
N CYCLES
T_n SECONDS
f_s
t
2^P
2y
f_{nx}
M_{min}
M_{max}
M_n
t
d_n
d_{n+1}
S_n
• --- INTEGER POINTS

FIG. 4


2
5
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9
RTS
COMPARATOR
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OUTPUT
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GATING
SIGNAL
t
M_1
AND
GATE
40
OUTPUT
t
S_n

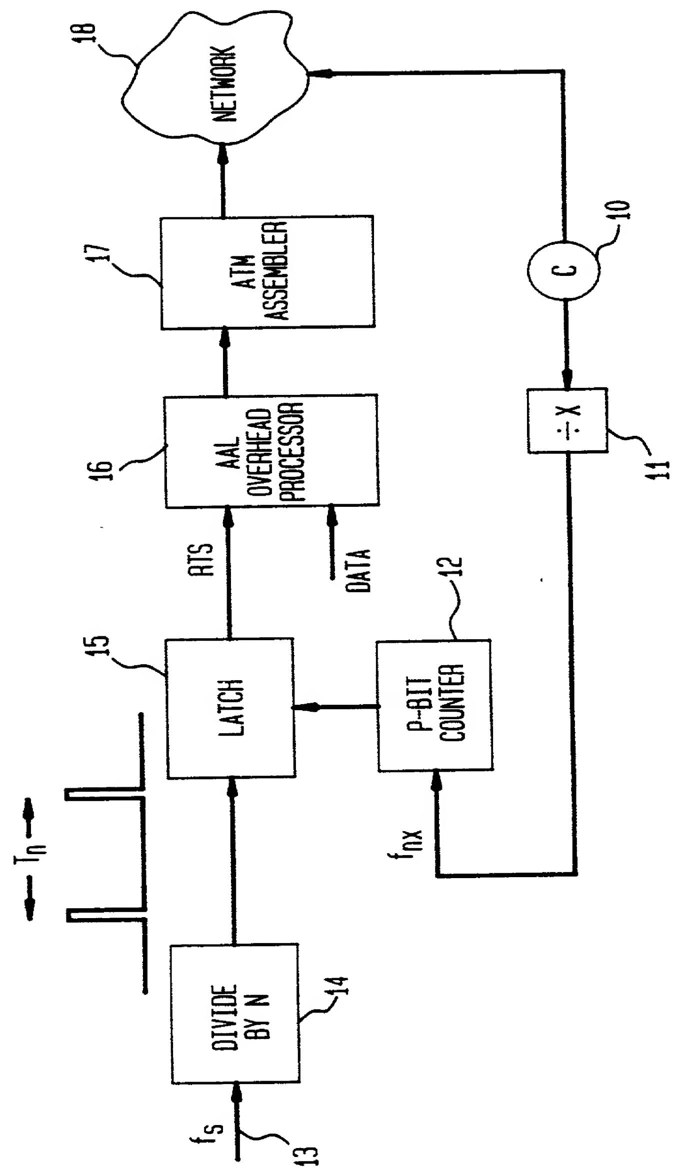
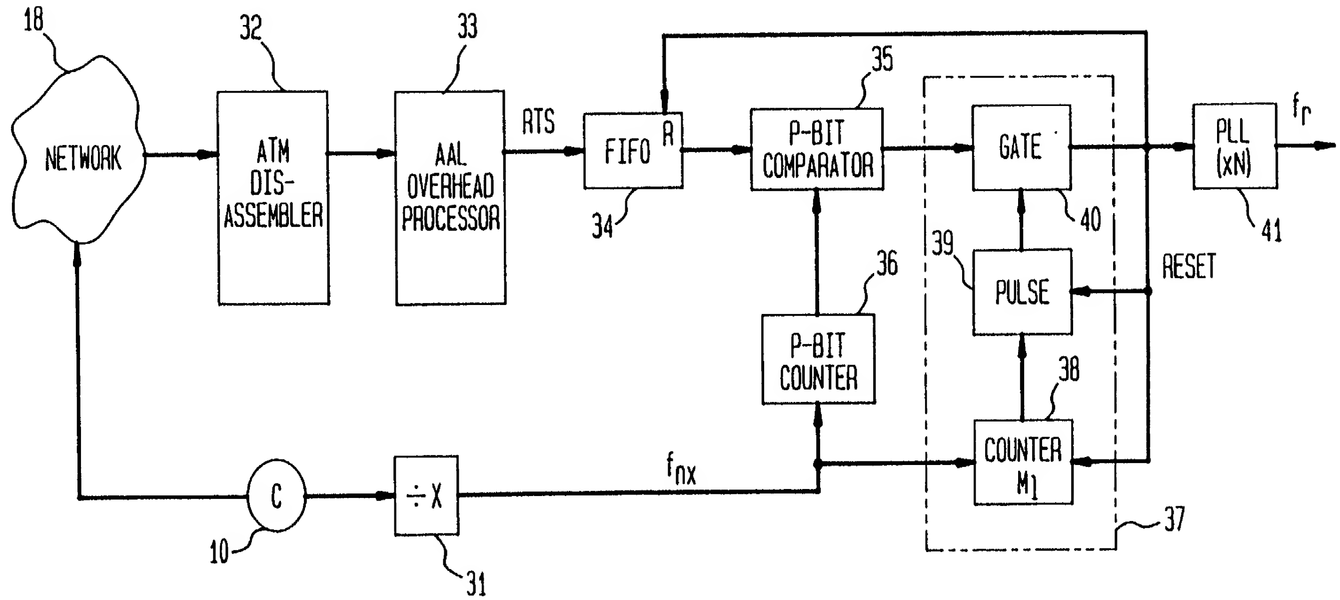

NETWORK
18
ATM
ASSEMBLER
17
AAL
OVERHEAD
PROCESSOR
16
RTS
DATA
LATCH
15
P-BIT
COUNTER
12
DIVIDE
BY N
14
f_S
13
T_n
f_{nx}
C
10
÷ X
11

FIG. 2

FIG. 3


18
NETWORK
32
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AAL
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PROCESSOR
RTS
FIFO
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34
35
P-BIT
COMPARATOR
36
P-BIT
COUNTER
GATE
40
39
PULSE
38
COUNTER
M1
37
PLL
(xN)
41
f_r
RESET
f_nx
C
10
÷X
31

PATENT
BOX REISSUE
Attorney Docket No.: 1333-0116

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of:	
U.S. Patent No. 5,260,978	
Patentees: Paul E. Fleischer et al.	
Issued: November 9, 1993	Group Art Unit: 2614
Serial No.: 07/969,592	Examiner: Hai H. Phan
Filed: October 30, 1992	
For: SYNCHRONOUS RESIDUAL TIME STAMP FOR TIMING RECOVERY IN A BROADBAND NETWORK	

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

ASSENT OF ASSIGNEE

Bell Communications Research, Inc., of the address given below, is the sole Assignee of United States Patent No. 5,260,978, granted on November 9, 1993, by an assignment executed by the inventors Paul E. Fleischer and Chi-Leung Lau and recorded in the U. S. Patent and Trademark Office on October 30, 1992 at Reel 6310, Frame 0008, and hereby assents to the reissue of United States Patent No. 5,260,978. The evidentiary documents have been reviewed and Assignee certifies that to the best of Assignee's knowledge and belief, title to the above-identified application is in Assignee.

I hereby declare that I am authorized to sign for Bell Communications Research, Inc. that all statements made herein of my own knowledge are true and that all statements made on

information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: 0 8 NOV 1995

Leonard Charles Suchyta, Esq.
Bell Communications Research, Inc.
Morris Corporate Center
445 South Street
Morristown, New Jersey 07960-6438